

CLAIMS

1 1. A parallel hardware-based multithreaded processor
2 comprises:

3 a general purpose processor that coordinates system
4 functions; and

5 a plurality of microengines that support multiple
6 hardware threads.

1 2. The processor of claim 1 wherein the general purpose
2 processor load microcontrol programs in the plurality of
3 microcontrol engines.

1 3. The processor of claim 1 further comprising a memory
2 control system.

1 4. The processor of claim 1 wherein the memory control
2 system comprises a synchronous dynamic random access memory
3 controller that sorts memory references based on whether the
4 memory references are directed to an even bank or an odd bank of
5 memory.

1 5. The processor of claim 1 wherein the memory control
2 system comprises a static random access memory controller that
3 optimizes memory references based upon whether the memory
4 references are read references or write references.

1 6. The processor of claim 1 wherein each of the plurality
2 of microengines employ hardware-based context swapping amongst a
3 plurality of threads that are independently executable within
4 each of the microengines.

1 7. The processor of claim 1 further comprising a high
2 speed bus interface that couples the processor to a communication
3 bus.

1 8. The processor of claim 1 further comprising a bus
2 interface that couples the processor to a computer system bus.

1 9. The processor of claim 1 further comprising an internal
2 bus arrangement to couple shared resources in the processor to
3 the plurality of microengines.

1 10. The processor of claim 9 wherein the internal bus
2 arrangement to couple shared resources, comprises:
3 a first bus to couple the general purpose processor to
4 the plurality of microengines.

1 11. The processor of claim 9 wherein the internal bus
2 arrangement to couple shared resources, comprises:
3 a translator device that translates requests from the
4 general purpose processor to the microengines; and
5 a first bus to couple the general purpose processor to
6 the plurality of microengines.

1 12. The processor of claim 3 wherein the internal bus
2 arrangement to couple shared resources, comprises:
3 a translator device that translates requests from the
4 general purpose processor to the microengines; and
5 a first bus to couple the general purpose processor to
6 the plurality of microengines; and
7 a second bus to couple the general purpose processor to
8 the memory control system.

1 13. The processor of claim 11, further comprising a third
2 bus to couple the microengines to external bus interfaces.

1 14. The processor of claim 8 wherein the shared resources
2 comprise:

3 a memory controller for controlling access to low
4 latency memory;
5 a memory controller for controlling an access to high
6 bandwidth memory;
7 a bus interface for controlling access to a
8 communications bus; and
9 a bus interface for controlling access to a computer
10 bus.

1 15. The processor of claim 1 wherein each one of the
2 microengines includes a program counter to uniquely identify a
3 position of a thread during execution in the microengine.

1 16. The processor of claim 1 wherein the processor supports
2 global signaling to each of the microengines.

1 17. The processor of claim 16 wherein the global signaling
2 is available to each thread in each microengine.

1 18. The processor of claim 17 wherein the global signaling
2 is available to each thread to permit each thread to take a
3 branch.

1 19. A parallel hardware-based multithreaded processor
2 comprises:
3 a general purpose processor that coordinates system
4 functions;

5 a plurality of microengines that support multiple
6 hardware threads;
7 a memory control system comprising:
8 a first memory controller that sorts memory references
9 based on whether the memory references are directed to an even
10 bank or an odd bank of memory; and
11 a second memory controller that optimizes memory
12 references based upon whether the memory references are read
13 references or write references.

1 20. The parallel hardware-based multithreaded processor of
2 claim 19 wherein the first memory controller controls synchronous
3 dynamic random access memory and the second memory controller
4 controls static random access static memory.